SpaceWire Margins Tester

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SpW performance degrading factors:

- **Evolutional:**
  - *Higher speeds*
  - *Longer distances*
  - *Lower Bit Error Rate (BER) levels requirements*
- **Physical media losses:**
  - *Smaller wire cross-section (to save weight)*
  - *Cable/connector parameters deviations and imperfections*
- **Interface hardware:**
  - *Parameters variations from different IC manufacturers*
- **External media susceptibility:**
  - *Common Mode Voltage (CMV) noise*
  - *Electro Magnetic Interference (EMI)*

Needed: verification tools to assess SpW margins!!

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Parts to be tested:

- **FPGA / ASIC**
  - *Digital simulation*
    - Standard design procedure
- **Transmitter**
  - *No testing except maximum drive current*
    - Fixed and specified by manufacturer
- **Receiver**
  - *Most likely to fail (induce errors) due to various operational conditions*
    - Marginal operation conditions needs to be established

Required: define marginal receiver operation conditions

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Parameters to be simulated:

- **Skew/Jitter:**
  - *Between Data and Strobe*
  - *Within each D/S pair*
- **Received signal span:**
  - *Guaranteed minimum Peak-to-Peak (P2P) voltage span at receiver end*
- **Common mode voltage:**
  - *Received signal bias*

Goal: simulate marginal receiver "eye" at desired BER or FER (Frame Error Rate)

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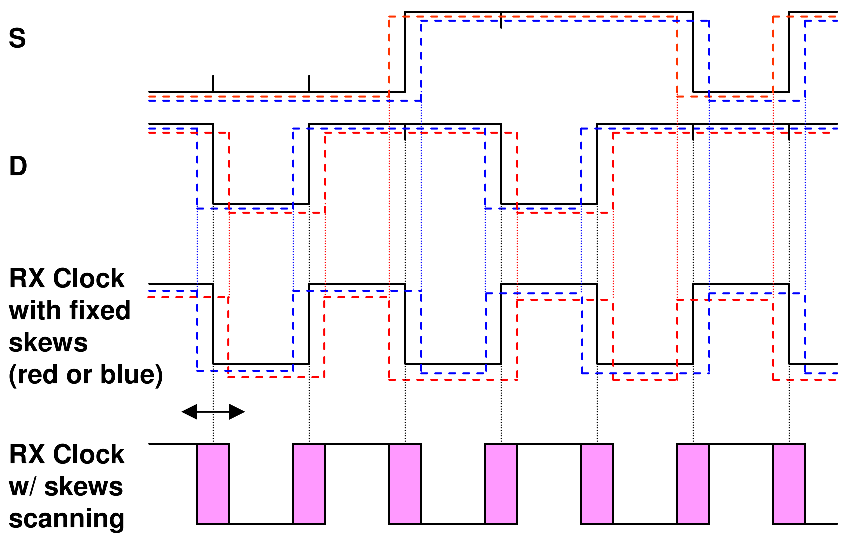
Parameter simulation diagrams:

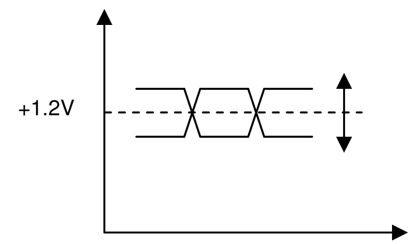
D/S skew



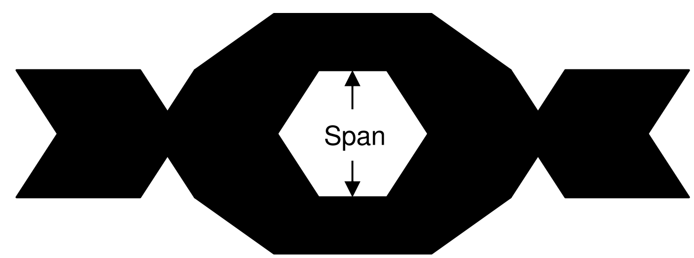
Red: fixed positive D / negative S skew

Blue: fixed negative D / positive S skew

LVDS bias



"Eye" span



Major SpW physical layer parameters can be simulated

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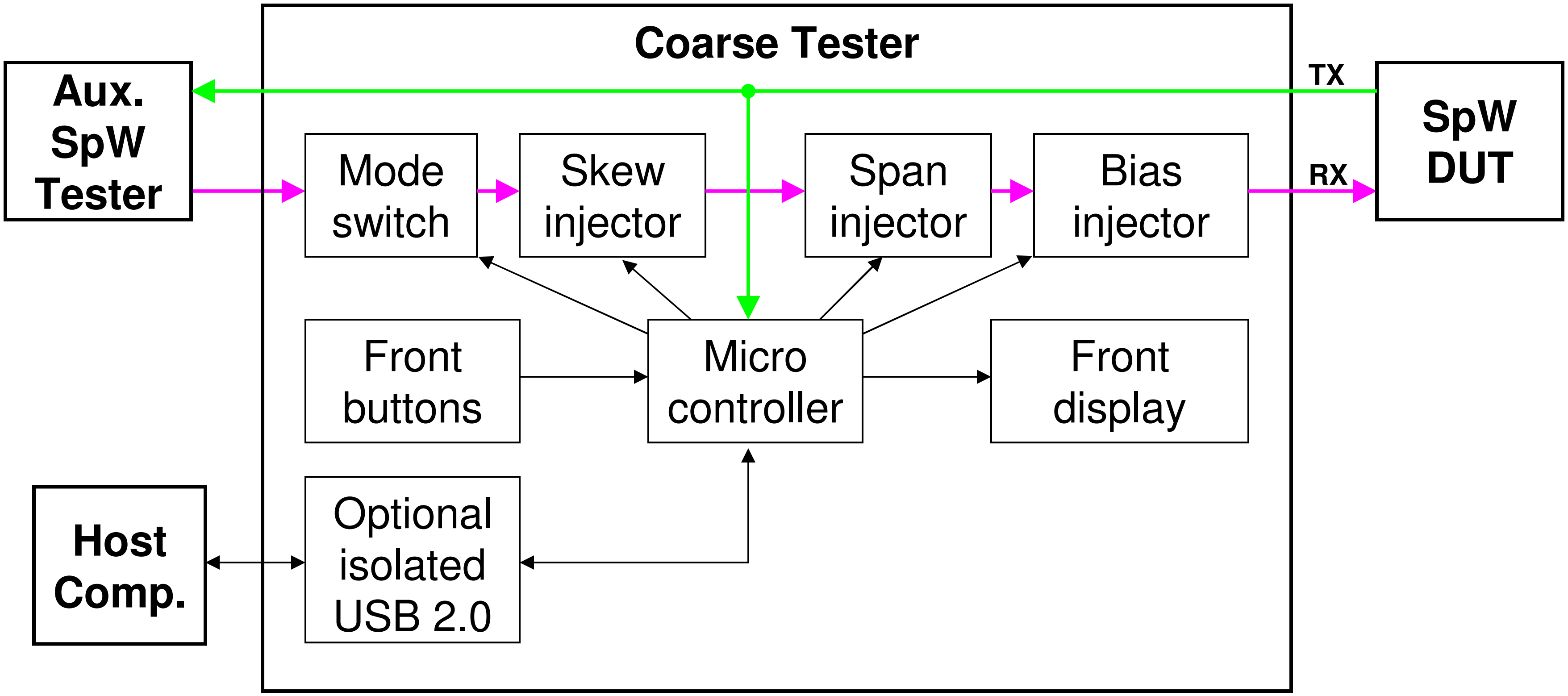
Suggested Tester types:

- **Coarse** (no effects on protocol or communication speed):
  - *Pass through mode:*
    - Inserted between known good SpW transmitter (Auxiliary Tester) and Device Under Test (DUT) receiver for full duplex peer-to-peer SpW operation
  - *Loop back mode:*
    - Connected to DUT as Slave and loops marginalized signal back to DUT
  - *Error detection:*
    - DUT SpaceWire dropouts monitoring
- **Precise** (simulates protocol and communication speeds):
  - *Master mode*:
    - Connected to DUT and works as Master
    - Emulates SpW protocol with simultaneous signal marginalization
  - *Error detection:*
    - Works as simple BER tester, assuming that DUT can report errors back to it
    - Dropouts monitoring as in Coarse tester

**Proposed: create 1 Coarse tester by Q4 2008;
start on Precise tester in Q1 2009**

Coarse tester diagram (<u>Pass</u> mode):



Full duplex communication between Master and DUT

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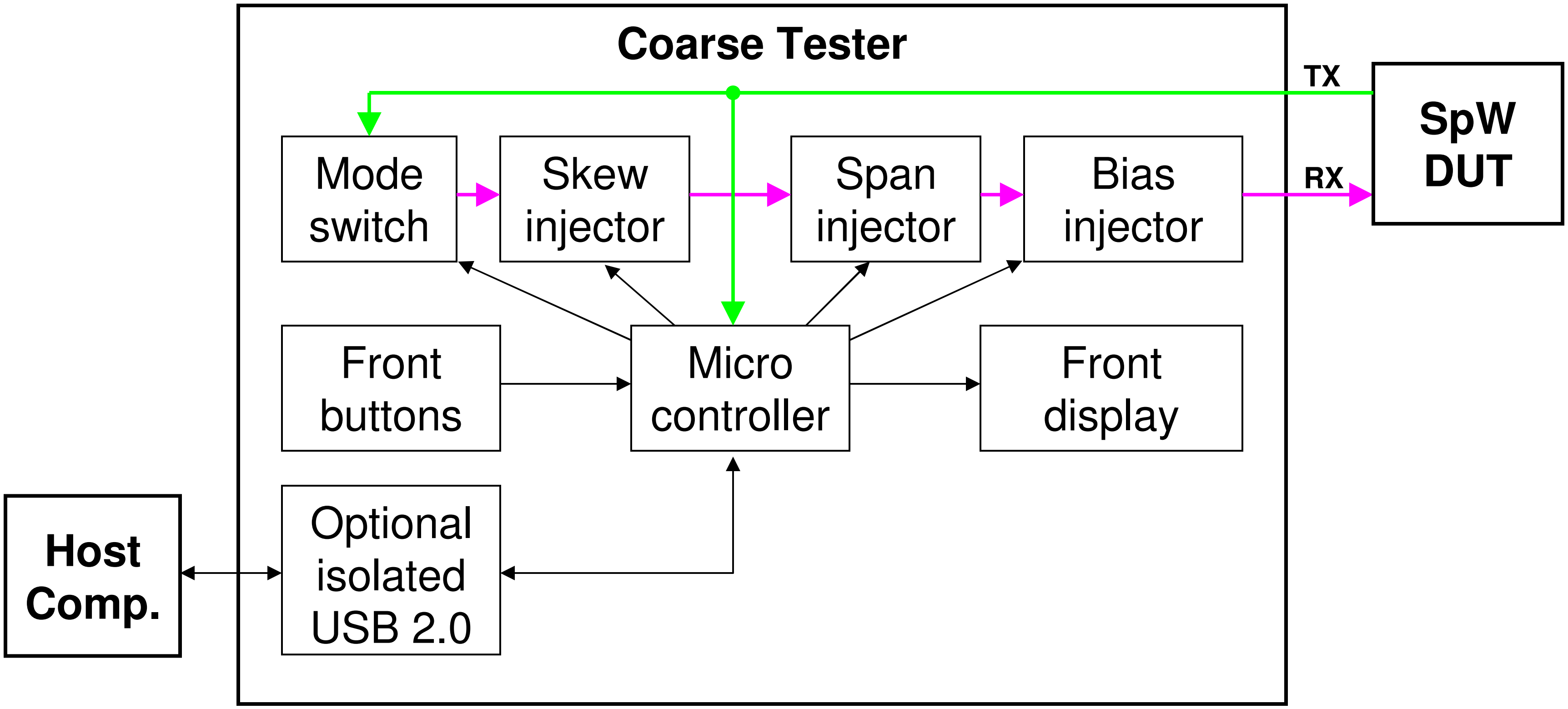
Coarse tester diagram (Loop mode):



Tester is used as "bend pipe" for DUT

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Coarse tester parameters for both Pass and Loop modes:

- **D and S Skew injection:**
  - ***Simulation range***
    - 0 to ±30 nS (speed dependent) from “0” nominal with D leading and S trailing, or vs. vs.; max of 61 steps
  - ***Internal differential pair skew injection:***
    - None
  - ***Step resolution***
    - 1 nS with ± 0.5 nS accuracy
- **Span injection:**
  - ***Simulation range***
    - 180–720 mV peak-to-peak at 100 Ohm termination
  - ***Step resolution***
    - 20 mV with ± 10 mV accuracy in 28 steps
- **Bias injection:**
  - ***Simulation range***
    - ± 1.2 V from +1.2 V LVDS nominal
  - ***Step resolution***
    - 200 mV with ± 10 mV accuracy in 13 steps
- **Other parameters:**
  - ***Operating speed***
    - 10 to 200 Mbps (with potential to 310 Mbps) in 20 (31) steps of 10 Mbps each
  - ***Number of stored test profiles***
    - up to 8
  - ***Protocol dropouts detection***
    - Up to 99999 over 99999 seconds (27+ hours)
  - ***Pin 3 (Transmit Ground) short to chassis detection and warning***
  - ***Dimensions (DxWxH):***
    - 160mm x 160mm x 86mm
  - ***Optional communications port***
    - Isolated USB 2.0

Most LVDS and SpW parameters are being covered

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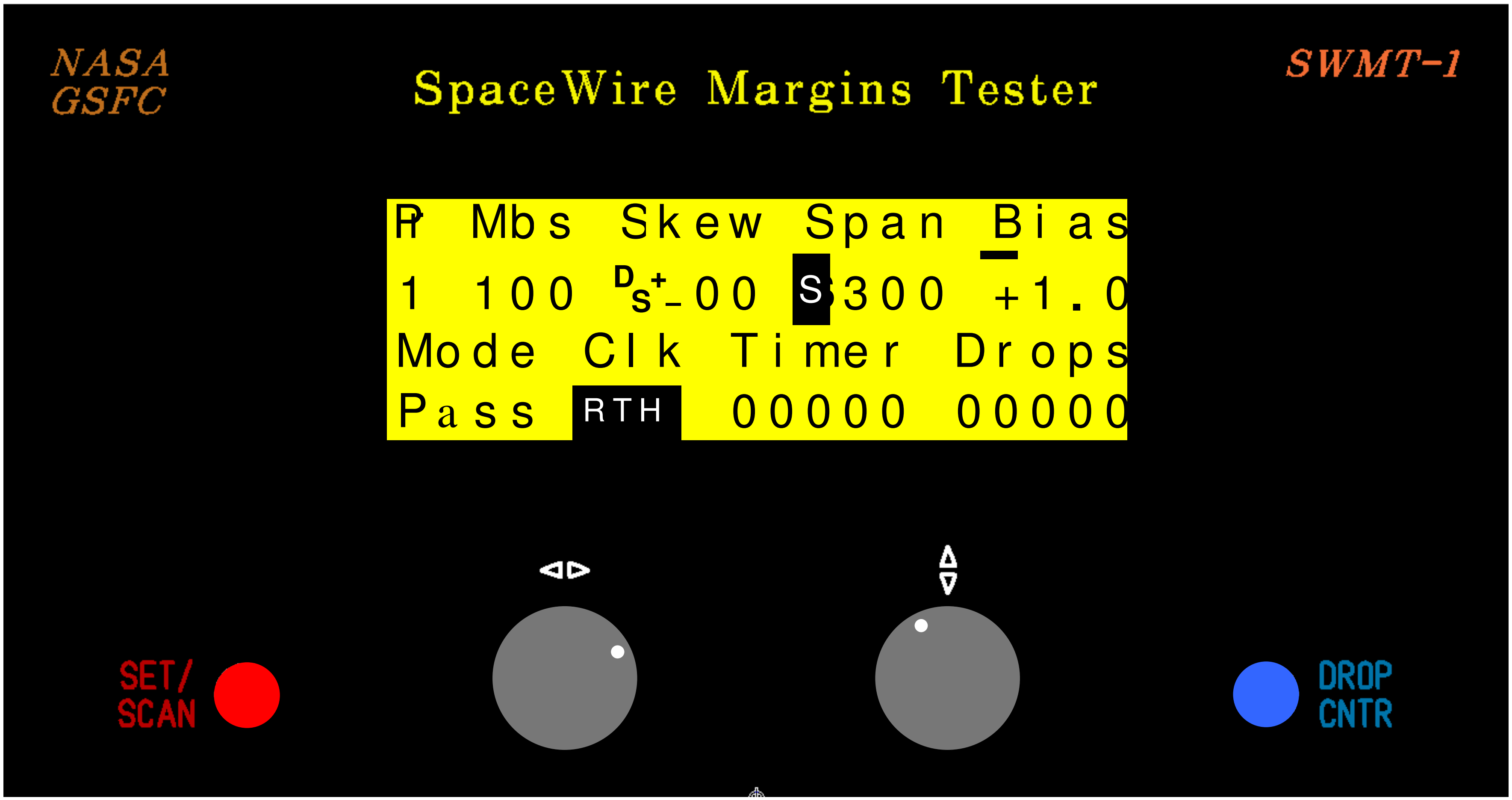
Coarse tester preliminary front panel appearance:



Stand alone portable unit

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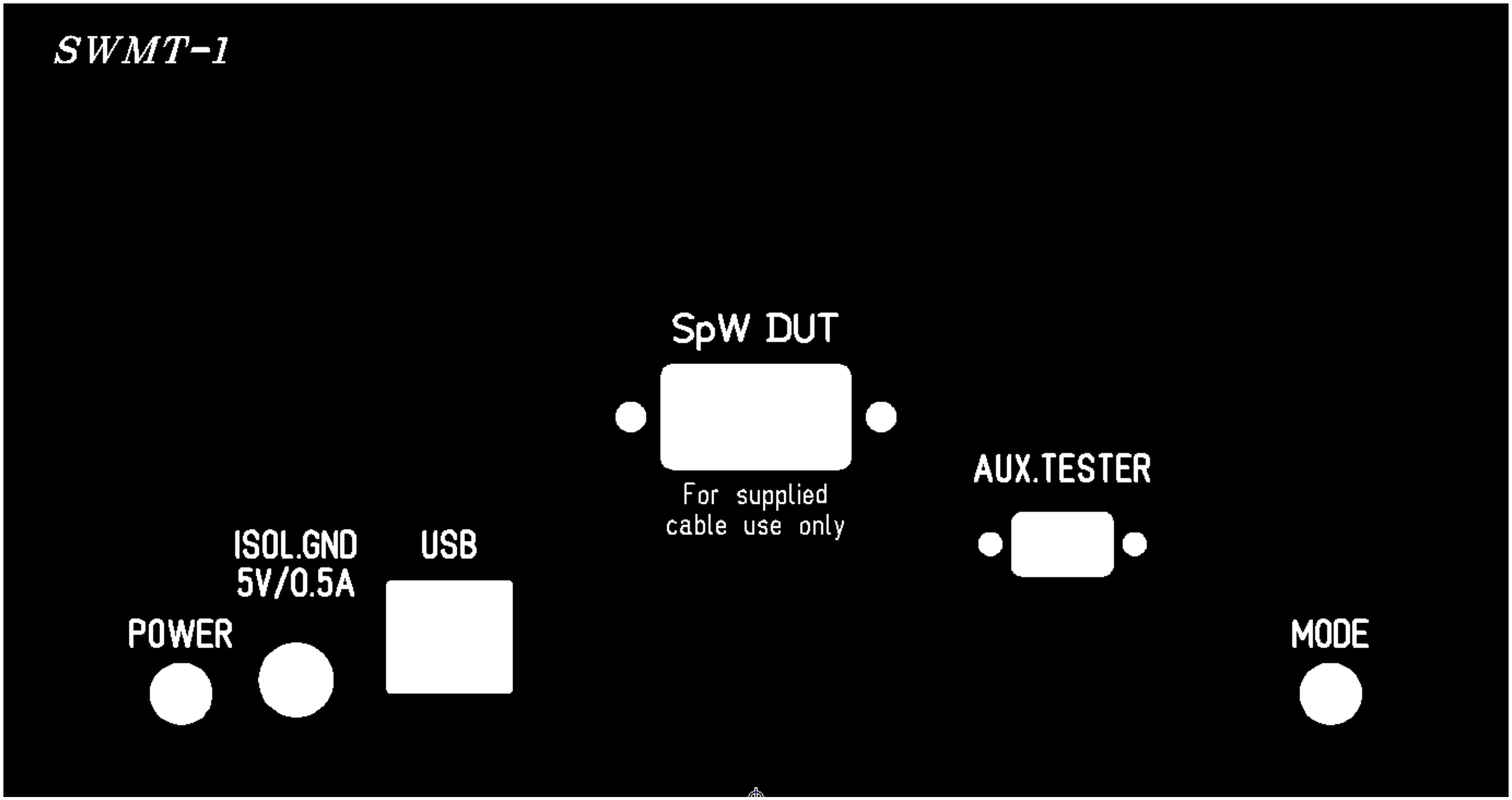
Coarse tester preliminary back panel appearance:



Optional USB port control

Coarse tester parameters control:

- **Horizontal encoder wheel:**
  - ***Selects between Profile, Mbps, Skew, Span, Bias fields***
- **Vertical encoder wheel:**
  - ***Selects between available values assigned to the above fields***
- **Scan button:**
  - ***Momentary press:***
    - Toggle Scan option for each individual field (Skew, Span, Bias)
  - ***1 sec press:***
    - Toggle Scan option for all 3 fields at a time regardless of currently selected field
- **Drop button:**
  - ***Momentary press:***
    - Start / Stop **Drops** counter and **Timer**
  - ***1 sec press:***
    - Reset **Drops** counter and **Timer**
- **Mode button:**
  - ***Switches between Loop and Pass modes***
- **USB port:**
  - ***Provides isolated ground communications with host computer***
    - Transmission
      - *Immediate report on any wheels / buttons changes*
      - *Immediate report on any changes of Drop counter with 1 ms quantization*
    - Reception
      - *New setup data and functions*

Simple interface

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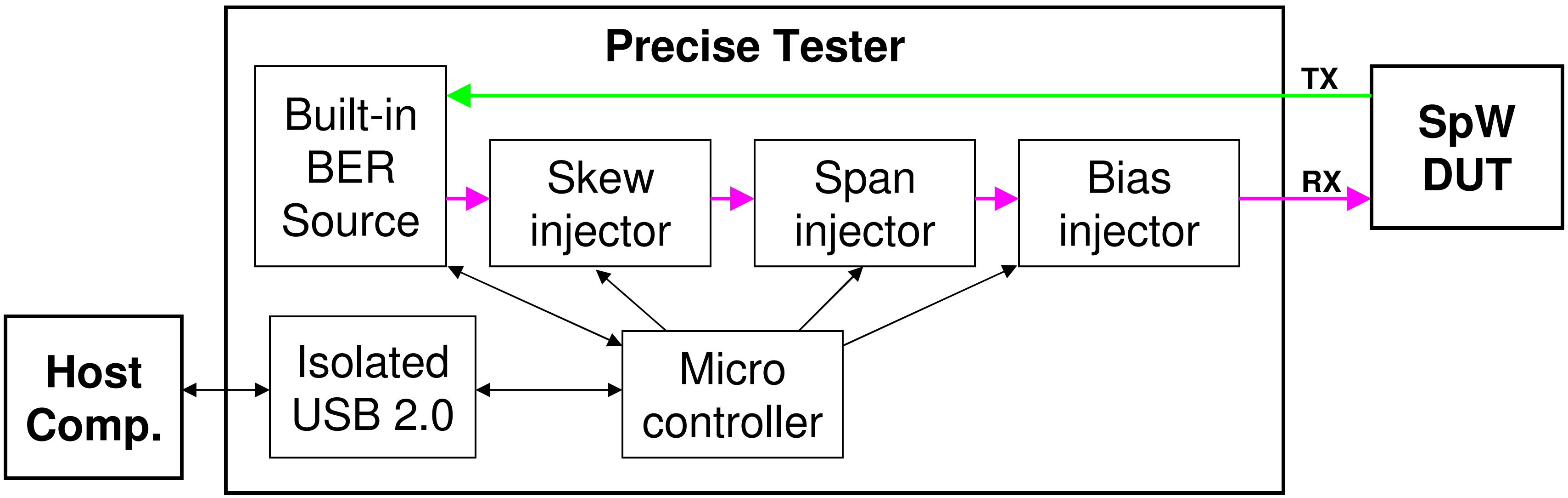
Precise tester diagram:



Tester will provide more comprehensive and automated DUT simulation

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Precise tester preliminary parameters:

- **D and S Skew injection:**
  - *Simulation range*
    - ±50 nS (speed dependent) from nominal
  - *Internal differential pair skew injection:*
    - ±1 nS
  - *Step resolution*
    - 0.2 nS ± 0.05 nS
- **Span injection:**
  - *Simulation range*
    - 180–720 mV peak-to-peak at 100 Ohm termination
  - *Step resolution*
    - 20 mV ± 10 mV
- **Bias injection:**
  - *Simulation range*
    - ± 1.2 V from +1.2 V LVDS nominal
  - *Step resolution*
    - 100 mV ± 10mV
- **Other parameters:**
  - *Maximum operating speed*
    - 400 Mbps (TBR)
  - *Number of stored test profiles*
    - No limitations

Major requirement: DUT suppose to have a way to report errors back to tester

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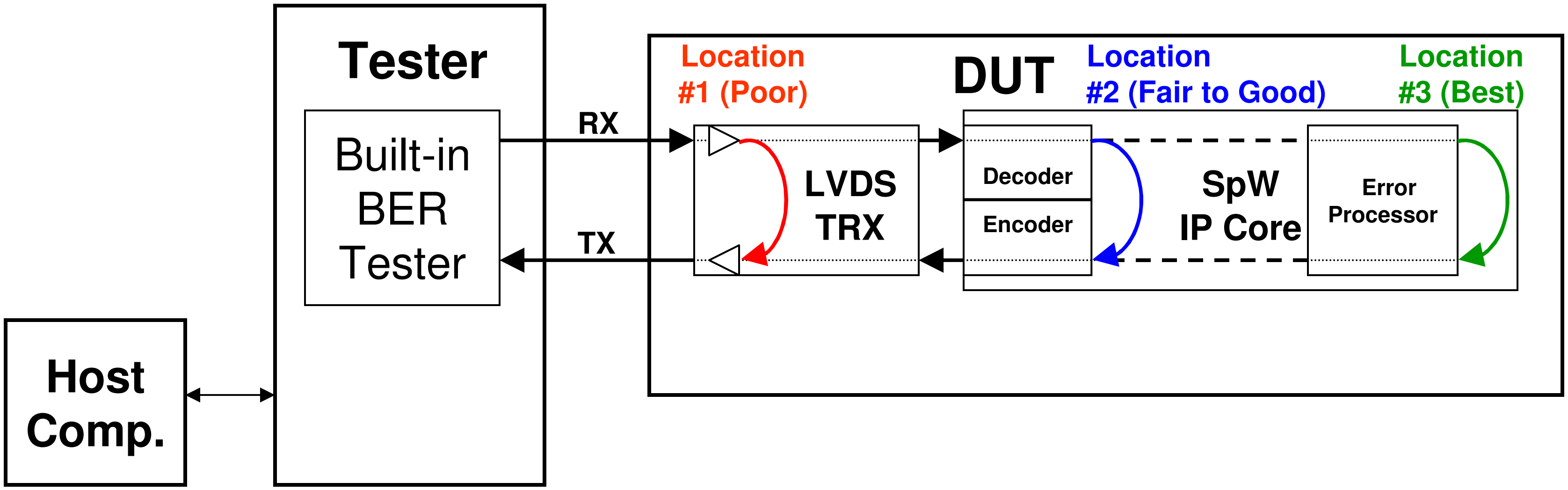
Precise tester error reporting locations diagram:



DUT might provide several locations for error reporting readbacks

Error reporting locations comparison:

- **Location #1 (on LVDS level such as in Aeroflex's PHY01 chip):**
  - ***Advantages***
    - Very simple implementation
  - ***Disadvantages***
    - Span and bias are corrected by LVDS receiver, skew is not corrected and is looped back exactly the same
    - BER is very poor and very imprecise
- **Location #2 (after SpW decoder and message processor with <u>minimum</u> core modifications):**
  - ***Advantages***
    - Simple implementation (just a loopback connection)
    - No special error registers
  - ***Disadvantages***
    - BER accountability is poor: possibility that only TX dropouts could be counted
- **Location #2 (after SpW decoder and message processor with <u>medium</u> core modifications):**
  - ***Advantages***
    - More complex implementation (loopback connection and protocol error registers to be reported on top of looped data)
    - Excellent BER accountability
  - ***Disadvantages***
    - Special codes in protocol: trying to differentiate error registers data in looped back data stream
    - High speed TX transmission: may induce more noise in RX data
- **Location #3 (after a special built-in error processor):**
  - ***Advantages***
    - Excellent BER accountability
    - Possible low speed TX rate: only received errors are transmitted back
    - Possibility of implementation of standard BER PRN sequences
  - ***Disadvantages***
    - New built-in function in SpW core

Different error reporting locations will yield different BER validity results

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Suggested requirements to DUT for better testing:

- **Built-in received errors counter**:
  - *General received error counter*
  - *Optional differentiation of error types*
- **Communication with DUT:**
  - *High speed receive rate from Tester to DUT*
  - *Preferable: fixed 10 Mbps error count transmit rate from DUT to Tester*
  - *Less preferable: injection of error results in to back data stream*
- **Error testing protocol:**
  - *Preferable: standard PRBS (PRN) from 2^7 -1 to 2^{15} -1 (only 1 is required)*
  - *Less preferable: standard SpW with new error codes*
- **Error display:**
  - *"Coarse" tester: counting SpW TX dropouts so it can be converted to BER*
  - *"Precise" tester: standard BER format fashion on remote test computer*

Added complexity enhances timing simulation and BER measurements